We claim:

1.   A method for processing data in a programmable processor, the method comprising:

decoding and executing instructions that instruct a computer system to perform operations,

5   at least some of the instructions including a group floating-point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands;

at least some group floating-point instruction being a group floating-point multiply-and-

10   add instruction, further operating on a third register partitioned into a plurality of floating-point operands,

operable to multiply the plurality of floating-point operands in the first and second registers and add the plurality of floating-point operands in the third register, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point

15   values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values.

2.   The method of claim 1,

.at least some group floating-point instruction being at least one member of the collection

20   consisting of group floating-point subtract, group floating-point add, and group floating-point multiply,

operable to perform a subtract, add and multiply respectively on the plurality of floating-point operands in the first and second registers, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being

represented by the defined result precision, and a catenated result having a plurality of

partitioned fields for receiving the plurality of floating point values; and

at least some group floating-point instruction being at least one member of the collection

consisting of group floating-point set less, and group floating-point set greater or equal,

5   operable to perform a set-less and set-greater-or-equal operation, respectively, on

the plurality of floating-point operands in the first and second registers, each producing a value

to provide a plurality of values, each of the values capable of being represented by the defined

result precision, and a catenated result having a plurality of partitioned fields for receiving the

plurality of values, wherein the value is zero if the operation produces a false result, and wherein

10   the value is an identity value if the operation produces a true result; and

at least some of the instructions comprising performing data manipulations on multiple

operands stored in partitioned fields of registers wherein the data manipulations comprise

copying or rearranging operands.

15   3.   The method of claim 2 wherein the zero value and the identity value are values that

construct a bit mask operable to select between alternate expressions using a bitwise Boolean

operation.

4.   The method of claim 1 wherein the catenated result has a width of 128 bits.

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5.   The method of claim 1 wherein the catenated result is provided to a register.

6.   The method of claim 1 wherein the defined precision is 16 bits.

7. The method of claim 1 wherein the defined precision is a format comprising one sign bit, five exponent bits and ten significand bits.

5 8. The method of claim 1 wherein the defined precision is 32 bits.

9. The method of claim 1 wherein the precision of the group floating-point instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits.

10 10. The method of claim 1 wherein the defined precision is 64 bits.

11. The method of claim 1 wherein the precision of the group floating-point instructions is a format comprising one sign bit, eleven exponent bits and 52 significand bits.

15 12. A computer-readable medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a group floating-point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable,

20 having a defined result precision which is equal to the defined precision of the operands;

at least some group floating-point instruction being a group floating-point multiply-and-add instruction, further operating on a third register partitioned into a plurality of floating-point operands,

operable to multiply the plurality of floating-point operands in the first and second

registers and add the plurality of floating-point operands in the third register, each producing a

floating-point value to provide a plurality of floating-point values, each of the floating-point

values capable of being represented by the defined result precision, and a catenated result having

5   a plurality of partitioned fields for receiving the plurality of floating point values.

13.   The computer-readable medium of claim 12,

at least some group floating-point instruction being at least one member of the collection

consisting of group floating-point subtract, group floating-point add, and group floating-point

10   multiply,

operable to perform a subtract, add and multiply respectively on the plurality of

floating-point operands in the first and second registers, each producing a floating-point value to

provide a plurality of floating-point values, each of the floating-point values capable of being

represented by the defined result precision, and a catenated result having a plurality of

15   partitioned fields for receiving the plurality of floating point values; and

at least some group floating-point instruction being at least one member of the collection

consisting of group floating-point set less, and group floating-point set greater or equal,

operable to perform a set-less and set-greater-or-equal operation, respectively, on

the plurality of floating-point operands in the first and second registers, each producing a value

20   to provide a plurality of values, each of the values capable of being represented by the defined

result precision, and a catenated result having a plurality of partitioned fields for receiving the

plurality of values, wherein the value is zero if the operation produces a false result, and wherein

the value is an identity value if the operation produces a true result; and

at least some of the instructions comprising performing data manipulations on multiple

operands stored in partitioned fields of registers wherein the data manipulations comprise

copying or rearranging operands.

5   14.   The computer-readable medium of claim 13 wherein the zero value and the identity value

are values that construct a bit mask operable to select between alternate expressions using a

bitwise Boolean operation.

15.   The computer-readable medium of claim 12 wherein the catenated result has a width of

10   128 bits.

16.   The computer-readable medium of claim 12 wherein the catenated result is provided to a

register

15   17.   The computer-readable medium of claim 12 wherein the defined precision is 16 bits.

18.   The computer-readable medium of claim 12 wherein the defined precision is a format

comprising one sign bit, five exponent bits and ten significand bits.

20   19.   The computer-readable medium of claim 12 wherein the defined precision is 32 bits.

20.   The computer-readable medium of claim 12 wherein the precision of the group floating-

point instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits.

21. The computer-readable medium of claim 12 wherein the defined precision is 64 bits.

22. The computer-readable medium of claim 12 wherein the precision of the group floating-

5 point instructions is a format comprising one sign bit, eleven exponent bits and 52 significand

bits.

23. A computer data signal, embodied in a transmission medium:

having instructions that instruct a computer system to perform operations,

10 at least some of the instructions including a group floating-point instruction operating on

first and second registers partitioned into a plurality of floating point operands, the floating point

operands having a defined precision and the defined precision being dynamically variable,

having a defined result precision which is equal to the defined precision of the operands;

at least some group floating-point instruction being a group floating-point multiply-and-

15 add instruction, further operating on a third register partitioned into a plurality of floating-point

operands,

operable to multiply the plurality of floating-point operands in the first and second

registers and add the plurality of floating-point operands in the third register, each producing a

floating-point value to provide a plurality of floating-point values, each of the floating-point

20 values capable of being represented by the defined result precision, and a catenated result having

a plurality of partitioned fields for receiving the plurality of floating point values.

24.   The computer data signal of claim 23,

at least some group floating-point instruction being at least one member of the collection consisting of group floating-point subtract, group floating-point add, and group floating-point multiply,

5   operable to perform a subtract, add and multiply respectively on the plurality of floating-point operands in the first and second registers, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values; and

10   at least some group floating-point instruction being at least one member of the collection consisting of group floating-point set less, and group floating-point set greater or equal,

operable to perform a set-less and set-greater-or-equal operation, respectively, on the plurality of floating-point operands in the first and second registers, each producing a value to provide a plurality of values, each of the values capable of being represented by the defined

15   result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of values, wherein the value is zero if the operation produces a false result, and wherein the value is an identity value if the operation produces a true result; and

at least some of the instructions comprising performing data manipulations on multiple operands stored in partitioned fields of registers wherein the data manipulations comprise

20   copying or rearranging operands.

25. The computer data signal of claim 24 wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using a bitwise Boolean operation.

5   26. The computer data signal of claim 23 wherein the catenated result has a width of 128 bits.

27. The computer data signal of claim 23 wherein the defined precision is 16 bits.

28. The computer data signal of claim 23 wherein the defined precision is a format
10   comprising one sign bit, five exponent bits and ten significand bits.

29. The computer data signal of claim 23 wherein the defined precision is 32 bits.

30. The computer data signal of claim 23 wherein the precision of the group floating-point
15   instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits.

31. The computer data signal of claim 23 wherein the defined precision is 64 bits.

32. The computer data signal of claim 23 wherein the precision of the group floating-point
20   instructions is a format comprising one sign bit, eleven exponent bits and 52 significand bits.